CLAIMS

[0063] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A photodiode for use in an imaging device, said photodiode comprising:

a charge collection region formed in a substrate of a first conductivity type for accumulating photo-generated charge, said charge collection region being of a second conductivity type and being adjacent a gate of a transistor formed over said substrate, said gate transferring charge accumulated in said charge collection region to a doped region of said second conductivity type; and

a doped layer of said first conductivity type, said doped layer being laterally displaced from an electrically active portion of said gate by a distance.

2. The photodiode of claim 1, wherein said distance is of about 100 to about 2,500 Angstroms.

3. The photodiode of claim 2, wherein said distance is of about 200 to about 1,000 Angstroms.

4. The photodiode of claim 1, wherein said doped layer is adjacent and in contact with an isolation region formed in said substrate.

5. The photodiode of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.

6. The photodiode of claim 5, wherein said doped layer is doped with a p-type dopant at a dopant concentration of from about 1 x 10^{17} to about 1 x 10^{19} atoms per cm^3.

7. The photodiode of claim 6, wherein said doped layer has a dopant concentration of from about 5 x 10^{17} to about 5 x 10^{18} atoms per cm^3.

8. The photodiode of claim 1, wherein said charge collection region is doped with an n-type dopant at a dopant concentration of from about 1 x 10^{16} to about 5 x 10^{17} atoms per cm^3.

9. The photodiode of claim 1, wherein said photodiode is one of a p-n-p photodiode or an n-p-n photodiode.

10. The photodiode of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.

11. The photodiode of claim 1, wherein said transistor is at least one of a transfer transistor, a reset transistor, a global shutter transistor, a high dynamic range transistor or a storage gate.

12. The photodiode of claim 1, wherein said imaging device is one of a 3T, 4T, 5T, 6T or 7T imaging device.

13. The photodiode of claim 1, wherein said imaging device is a CMOS imager.

14. The photodiode of claim 1, wherein said imaging device is a CCD imager.

15. An image pixel comprising:

a gate structure of a transistor formed over a semiconductor substrate; and

a photodiode adjacent said gate, said photodiode comprising a surface layer of a first conductivity type and a doped region of a second conductivity type located below said surface layer, said surface layer being laterally displaced from an electrically active portion of said gate by a distance of about 100 to about 2,500 Angstroms.

16. The image pixel of claim 15, wherein said surface layer is laterally displaced from said gate by a distance of about 200 to about 1,000 Angstroms.

17. The image pixel of claim 15, wherein said surface layer is doped with a p-type dopant at a dopant concentration of from about 1×10^{17} to about 1×10^{19} atoms per cm^3.

18. The image pixel of claim 17, wherein said surface layer has a dopant concentration of from about 5×10^{17} to about 5×10^{18} atoms per cm^3.

19. A CMOS image sensor comprising:

a semiconductor substrate;

an isolation region formed within said semiconductor substrate; and

a pixel adjacent said isolation region, said pixel comprising a photodiode adjacent a gate of a transistor, said photodiode further comprising a surface layer of a first conductivity type and a doped region of a second conductivity type located below said surface layer, said surface layer being laterally displaced from an electrically active portion of said gate by a distance of about 100 to about 2,500 Angstroms.

20. The CMOS image sensor of claim 19, wherein said surface layer is laterally displaced from said gate of said transistor by a distance of about 200 to about 1,000 Angstroms.

21. The CMOS image sensor of claim 19, wherein said surface layer is adjacent and in contact with said isolation region.

22. The CMOS image sensor of claim 19, wherein said first conductivity type is p-type and said second conductivity type is n-type.

23. The CMOS image sensor of claim 19, wherein said surface layer is doped with boron or indium.

24. The CMOS image sensor of claim 19, wherein said surface layer is doped with a p-type dopant at a dopant concentration of from about 1×10^{17} to about 1×10^{19} atoms per cm^3.

25. The CMOS image sensor of claim 24, wherein said surface layer has a dopant concentration of from about 5 x 10^{17} to about 5 x 10^{18} atoms per cm^3.

26. The CMOS image sensor of claim 19, wherein said photodiode is a p-n-p photodiode.

27. The CMOS image sensor of claim 19, wherein said photodiode is an n-p-n photodiode.

28. The CMOS image sensor of claim 19, wherein said transistor is one of a transfer transistor or a reset transistor.

29. A CMOS image sensor comprising:

a silicon substrate;

a field oxide region formed within said silicon substrate; and

a pixel adjacent said field oxide region, said pixel comprising a p-n-p photodiode adjacent a gate of a transistor, said p-n-p photodiode further comprising a p-type surface layer and an n-type doped region located below said p-type surface layer and relative to said p-type surface layer, said p-type surface layer being laterally displaced from said gate by a distance of about 100 to about 2,500 Angstroms.

30. The CMOS image sensor of claim 29, wherein said p-type surface layer is laterally displaced from said gate by a distance of about 200 to about 1,000 Angstroms.

31. The CMOS image sensor of claim 29, wherein said p-type surface layer is adjacent and in contact with said field oxide region.

32. The CMOS image sensor of claim 29, wherein said p-type surface layer and said n-type doped region are both located within a p-type doped region.

33. The CMOS image sensor of claim 29, wherein said p-type surface layer is doped with a dopant at a dopant concentration of from about 1×10^{17} to about 1×10^{19} atoms per cm^3.

34. The CMOS image sensor of claim 33, wherein said p-type surface layer has a dopant concentration of from about 5×10^{17} to about 5×10^{18} atoms per cm^3.

35. The CMOS image sensor of claim 29, wherein said transistor is one of a transfer transistor or a reset transistor.

36. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:

a substrate; and

a photo-collection region including a first type material region at junction with a second type material layer, the first type material region being located at least under a portion of a gate of a transistor, said second

type material layer being spaced at a surface of said substrate from said first type material region by a distance of about 100 to about 2,500 Angstroms.

37. The CMOS imager system of claim 36, wherein said first type material region is an n-type region and said second type material layer is a p-type layer.

38. The CMOS imager system of claim 36, wherein said transistor is one of a transfer transistor or a reset transistor.

39. A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming at least one isolation region in a substrate;

forming a gate of a transistor over said substrate, said gate being spaced apart from said at least one isolation region;

forming a first doped layer of a first conductivity type in said substrate;

forming a doped region of a second conductivity type in said doped layer; and

forming a second doped layer of said first conductivity type in said substrate by implanting ions of said first conductivity type at an incidence angle with said substrate different than a zero degree angle in an area of said substrate defined between said gate and said at least one isolation region, said gate acting as an implant mask for said incidence angle, said second doped layer being in contact with said isolation region and being

displaced laterally from an electrically active portion of said gate by a distance.

40. The method of claim 39, wherein said second doped layer is laterally displaced from said electrically active portion of said gate by about 100 to about 2,500 Angstroms.

41. The method of claim 39, wherein said second doped layer is laterally displaced from said electrically active portion of said gate by about 200 to about 1,000 Angstroms.

42. The method of claim 39, wherein said first conductivity type is p-type and said second conductivity type is n-type.

43. The method of claim 39, wherein said act of forming said doped region of said second conductivity type further comprises forming a photoresist layer over said substrate and said gate, and patterning said photoresist layer to expose said area of said substrate located between said gate and said at least one isolation region.

44. The method of claim 43, wherein said angle of said implanting is of about 3 degrees to about 40 degrees.

45. The method of claim 44, wherein the height of said gate is of about 400 Angstroms to about 4,000 Angstroms and the thickness of said photoresist layer is of about 1,000 Angstroms to about 10,000 Angstroms.

46. The method of claim 39, wherein said act of implanting ions of said first conductivity type further comprises directing a dopant at said incidence angle which is different than a zero degree angle in said area of said substrate located between said gate and said at least one isolation region.

47. The method of claim 39, wherein said photodiode is formed as a p-n-p photodiode.

48. A method of forming a p-n-p photodiode for a CMOS imaging device, said method comprising:

forming at least one field oxide region in a silicon substrate;

forming a transistor gate over said silicon substrate and spaced apart from said at least one field oxide region;

forming an n-type doped region in said silicon substrate by implanting n-type ions at an incidence angle with said silicon substrate other than ninety degrees;

forming an insulating layer over said transistor gate and said silicon substrate; and

forming a p-type doped layer within said silicon substrate and above said n-type doped region, said p-type doped layer being in contact with said isolation region and being displaced laterally from an electrically active area of said transistor gate by a distance, said p-type doped layer

having a dopant concentration within the range of from about 1 x 10^{17} to about 1 x 10^{19} atoms per cm^3.

49. The method of claim 48, wherein said p-type doped layer is laterally displaced from said electrically active area of said transistor gate by about 100 to about 2,500 Angstroms.

50. The method of claim 48, wherein said p-type doped layer is laterally displaced from said electrically active area of said transistor gate by about 200 to about 1,000 Angstroms.

51. The method of claim 48, wherein said act of forming said p-type doped layer further comprises implanting p-type ions at an incidence angle with said silicon substrate other than zero degrees.

52. The method of claim 48, wherein said act of forming said p-type doped layer further comprises implanting p-type ions at an incidence angle with said silicon substrate of about zero degrees.

53. The method of claim 48, wherein said act of forming said n-type doped region further comprises forming a photoresist layer over said silicon substrate and said gate.

54. The method of claim 53, wherein said act of forming said n-type doped region further comprises patterning said photoresist layer to expose an area of said silicon substrate

located between said transistor gate and said at least one isolation region.

55. The method of claim 54, wherein said photoresist layer is formed to a thickness of about 1,000 Angstroms to about 10,000 Angstroms.

56. The method of claim 55, wherein said implanting act is conducted at an angle of about 3 degrees to about 40 degrees.

57. The method of claim 56, wherein the height of said transistor gate is of about 400 Angstroms to about 4,000 Angstroms.

58. The method of claim 48, wherein said n-type doped region has a dopant concentration within the range of from about 1×10^{16} to about 5×10^{17} atoms per cm^3.

59. A method of forming a p-n-p photodiode for a pixel sensor cell, said method comprising:

forming at least one field oxide region in a substrate;

forming a transistor gate over said substrate and spaced apart from said at least one field oxide region;

forming a first p-type doped layer in said substrate;

forming a photoresist layer over said transistor gate and said field oxide region;

patterning said photoresist layer to form an opening extending between a first location and a second location, said first location corresponding to a first point over said transistor gate and said second location corresponding to a second point over said field oxide region;

conducting a first implant through said opening to form an n-type doped region in said first p-type doped layer; and

conducting an angled implant through said opening to form a second p-type doped layer in said first p-type doped layer, said second p-type doped layer being located above said n-type doped region and laterally spaced thereof at a surface region of said substrate.

60. The method of claim 59, wherein said second p-type doped layer is formed in contact with said isolation region.

61. The method of claim 59, wherein said second p-type doped layer is displaced laterally from an electrically active area of said transistor gate by a distance.

62. The method of claim 59, wherein said second p-type doped layer is laterally displaced from said electrically active area of said transistor gate by about 100 to about 2,500 Angstroms.

63. The method of claim 59, wherein said second p-type doped layer has a dopant concentration within the range of from about 1×10^{17} to about 1×10^{19} atoms per cm^3.

64. The method of claim 59, wherein said photoresist layer is formed to a thickness of about 1,000 Angstroms to about 10,000 Angstroms.

65. The method of claim 64, wherein said angle of said angled implant is of about 3 degrees to about 40 degrees.

66. The method of claim 65, wherein the height of said transistor gate is of about 400 Angstroms to about 4,000 Angstroms.

67. A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming at least one isolation region in a substrate of a first conductivity type;

forming a gate of a transistor over said substrate, said gate being spaced apart from said at least one isolation region;

conducting a first angled implant to form a doped region of a second conductivity type in said substrate; and

conducting a second angled implant to form a doped layer of said first conductivity type in said substrate by implanting ions of said first conductivity type at an incidence angle with said substrate different than a zero degree angle in an area of said substrate defined between said gate and said at least one isolation region, said gate acting as an implant mask for said incidence angle, said doped layer being in contact with said

isolation region and being displaced laterally from an electrically active portion of said gate by about 100 to about 2,500 Angstroms.

68. The method of claim 67, wherein said doped layer is laterally displaced from said electrically active portion of said gate by about 200 to about 1,000 Angstroms.

69. The method of claim 67, wherein said act of conducting said second angled implant further comprises forming a photoresist layer over said substrate and said gate, and patterning said photoresist layer to expose said area of said substrate located between said gate and said at least one isolation region.

70. The method of claim 69, wherein said act of conducting said second angled implant further comprises directing ions of said first conductivity type at an incidence angle with said substrate which is different than a ninety degree angle in said area of said substrate located between said gate and said at least one isolation region.

71. The method of claim 70, wherein said incidence angle is of about 3 degrees to about 40 degrees.

72. The method of claim 71, wherein the height of said gate is of about 400 Angstroms to about 4,000 Angstroms and the thickness of said photoresist layer is of about 1,000 Angstroms to about 10,000 Angstroms.

73. The method of claim 67, wherein said act of conducting said first angled implant further comprises directing ions of said second conductivity type at an incidence angle with said substrate which is different than a zero degree angle.